Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**A**

**C**

**.036”**

**.036”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size:**

**Backside Potential: CATHODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .036” X .036” DATE: 11/4/21**

**MFG: MICROSEMI / CDI THICKNESS .000” P/N: 1N4765**

**DG 10.1.2**

#### Rev B, 7/1